Portability in the Signal Processing Subsystem

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What is the Problem?

- SCA Achieves Portability Goals Using CORBA to Isolate Waveform Applications from Processor
 - Extendible to DSPs with some penalties
 - Not applicable to FPGAs
- High Performance Waveforms and Space Environment Drive Solutions to Use DSPs & FPGAs
- Different DSPs optimized for different processing functions
 - Fixed-point vs. Floating-point
 - Device-unique instruction sets
 - Limited availability of CORBA ORBs
 - Use of OS and CORBA makes for heavy-weight footprint
- FPGA Technology Not Suited for Small Form Fit Radios
 - Large Size; High Power Draw; Cannot Turn Off Device to Save Power
 - ASIC Best Low Power Solution; Not Software Reconfigurable





What is the Vision of the Future?

- All Processing Elements Have Portable Waveform Software
 - Hardware Independent
 - Higher Order Language
 - Open Architecture Platforms Provide Standard Interfaces
 - Little or No Modification for Porting to New Platforms
- Platform / Waveform Constraints Affect the Balance
 - Robust and Complex Waveforms
 - Long Battery Life
 - Small Size
 - Radiation Environment





Challenges of Attaining the Vision

Near-Term Challenges

- Waveforms Still Hardware Specific (Modem)
- Typical Hardware Technology Large and Power Hungary
- Concerns Exist for Porting JPO Library Waveform Modem Code
 - Waveform Resource Utilization Untested
 - Risk moving forward with new designs
 - Low Power, Small Size Diminish Design Margin
 - Possible Limited use of Object-Oriented Design and Coding?
 - Standard Open Source Middleware Not Available for Porting

Far-Term Challenges

- Waveform Software Complexity Increasing, Requiring More Signal Processing Power
- General Purpose Processors Increasing MIPS, Size and Power Consumption
- Higher Order Languages and Representations Continually Evolving





Proposed Solutions for Meeting the Challenges

- Open Architecture Standards Within Modem
 - CORBA in DSP
 - Allow Migration of Processing from GPPs
 - Consider Less Than Full CORBA ORB/Naming Service/Event Service/Log Service
 - Hardware Abstraction Layer
 - Standardize on APIs for Significant Architectural Blocks
 - Signal Processing Functions
 - RF Interface and Control
 - BIT and Performance Monitoring
 - APIs Include Performance, Not Just Interface
 - Latency
 - Throughput
 - Jitter
 - Precision





Proposed Solutions for Meeting the Challenges

- Open Architecture Standards Within Modem, cont'd
 - Focus on Waveform Definition, Not Implementation
 - Every FPGA/ASIC Waveform Designer Provides
 - Block diagram or functional partitioning
 - RTL source code
 - Behavioral test benches on an Industry Standard Tool Set
 - Simulation tool, version, results and performance margins
 - Code coverage analysis statistics, if any
 - Technology dependent code, if any
 - Technology dependent IP cores, if any
 - Synthesis tool, version and implementation constraints
 - Place and Route tool, version and implementation constraints
 - Previously targeted device part number and logic utilization report



